CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. A method of adjusting carrier mobility in semiconductor devices comprising the steps of

depositing a metal or combination of metals to contact one of a first or second transistor gate structure, and

alloying said metal and said transistor gate structure to form a first stressed alloy within said transistor gate whereby a first stress is created in at least one corresponding channel of said first or second transistors without producing a stress in at least one channel of the other transistor of said first or second transistors.

2. A method as recited in claim 1 in which said alloy is a silicide.

3. A method as recited in claim 1 in which first transistor and second transistor are of opposite conductivity types.

4. A method as recited in claim 3 comprising further the steps of

depositing a metal over said first transistor gate and not over said second transistor gate to alloy with a first electrode to form said first stressed alloy causing a first stress to be applied in at least one channel of said first transistor, and

depositing a metal over said second transistor gate and not over said first transistor gate to alloy with a second electrode to form a second stressed alloy causing a second stress to be applied in at least the channel of said second transistor.

5. A method as recited in claim 4 in which said first stressed alloy and second stressed alloy apply opposing stresses.

6. A method as recited in claim 5 in which

said first stress caused by said first stressed alloy exhibits stress in at least the channel region of said first transistor opposite to the stress provided by said first stressed alloy, and

said second stress caused by said second stressed alloy exhibits stress in at least the channel region of said second transistor opposite to the stress provided by said second stressed alloy.

7. A method as recited in claim 6 wherein the carrier mobility is regulated by applying tensile stress to at least one channel of said first transistor while applying compressive stress to at least one channel of said second transistor.

8. A method as recited in claim 1 wherein said depositing step comprises

depositing a first metal to a portion of said gate electrode material in said first transistor to form a third alloy at the lower region of the gate electrode proximate to the channel of said first transistor; and

depositing a second metal over said first

transistor gate electrode to form said first stressed alloy within first transistor gate in the upper region of the gate electrode.

9. A method as recited in claim 8 wherein said depositing step further comprises

depositing a third metal to a portion of said gate electrode material in said second transistor to form a fourth alloy at the lower region of the gate electrode proximate to the channel of said second transistor; and

depositing a fourth metal over said second transistor gate electrode to form said second stressed alloy within second transistor gate in the upper region of the gate electrode, whereby said second stressed alloy creates a second stress to the channel area of said second transistor.

10. A method as recited in claim 9 wherein the first stressed alloy and second stressed alloy are of opposing stresses.

11. A method as recited in claim 10 wherein the first transistor and second transistor are of opposite conductivity types.

12. A method as recited in claim 11 wherein

said first transistor is an nFET wherein said first stressed alloy is compressive creating said first stress wherein first stress is tensile, and

said second transistor is a pFET wherein said second stressed alloy is tensile creating said second stress wherein second stress is compressive.

13. An apparatus that adjusts carrier mobility in semiconductor devices comprising:

a substrate,

a first transistor having a gate dielectric, gate electrode, and source, drain, and gate regions, formed on said substrate,

a second transistor having a gate dielectric, gate electrode, and source, drain, and gate regions, formed on said substrate, and

a first stressed alloy providing tensile stress at least in one channel of first transistor.

14. An apparatus as recited in claim 13 in which said alloy is a silicide.

15. An apparatus as recited in claim 13 further comprising a second stressed alloy providing compressive stress at least in one channel of second transistor.

16. An apparatus as recited in claim 15 wherein said first and second stressed alloys can be composed of SiNi, $CoSi_2$, PdSi, or other material that exhibits either tensile or compressive properties.

17. An apparatus as recited in claim 16 further comprising:

a third alloy located in the lower region of the gate area of said first transistor, and

a fourth alloy located in the lower region of the gate area of said second transistor.

18. An apparatus as recited in claim 17 in which

the gate electrode wraps around at least two sides of said channel of each of said first and second transistors.

19. An apparatus as recited in claim 13 wherein the first stressed alloy can be composed of SiNi, $CoSi_2$, PdSi, or other material that exhibits either tensile or compressive properties.

20. An apparatus as recited in claim 19 in which the gate electrode wraps around at least two sides of said channel of each of said first and second transistors.